On-chip optical detectors in Standard CMOS SOI

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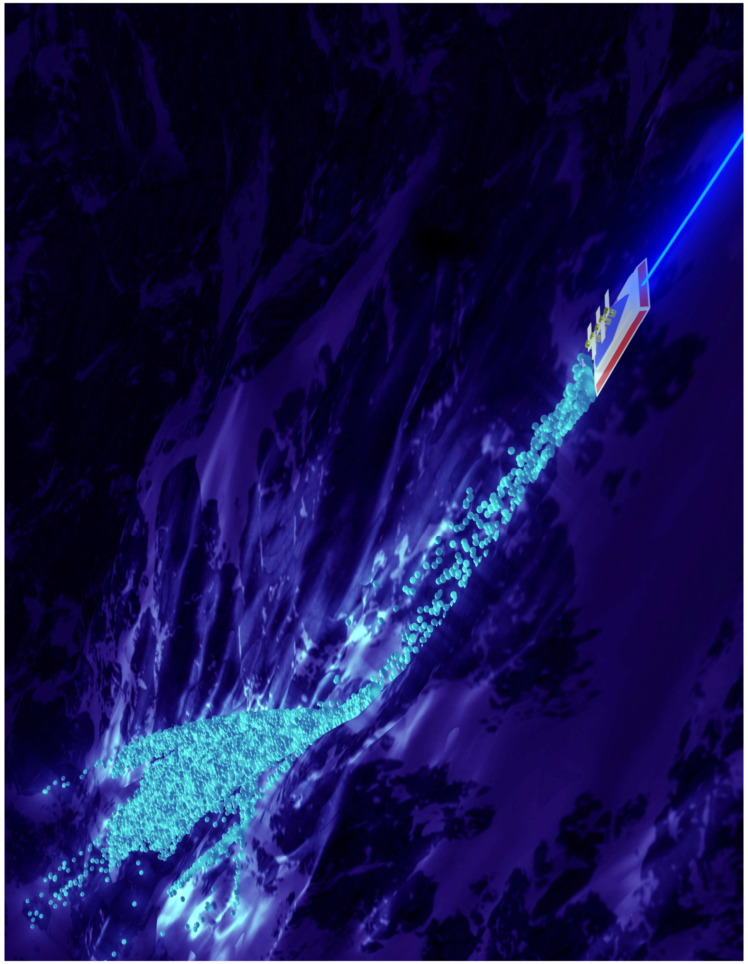


Visualization of the avalanche effect in avalanche photo-detectors

Outline

- Motivation
- Electrical and Optical Interconnects
- Silicon Photonics
- Optical detectors in Standard CMOS
  - Poly-Silicon Grating
  - Shallow-Trench-Isolation Grating
  - Germanium Waveguide
- Summary and Outlook

Motivation

- Significant annual growth in demand for network bandwidth
  - High-speed broadband
  - High-definition (HD) Video/TV
  - Consumer IP
  - Social media
  - Cloud computing
  - ...
- Increasing gap between network traffic and hardware I/O bandwidth
  - Bandwidth demand doubles every 18 month [1]
  - Server bandwidth doubles every 24 months [1]
- Electrical interconnect performance stagnates since several CMOS generations (Fig. 1+2)

[1] Proceedings of the IBM Printed Circuit Board Symposium, Raleigh, USA, 2011

[2] G. Chen et al., „Electrical and Optical On-Chip Interconnects in Scaled Microprocessors“, Proceedings of the IEEE International Symposium on Circuits and Systems, Vol. 3, pp. 2514-2517, 2005.

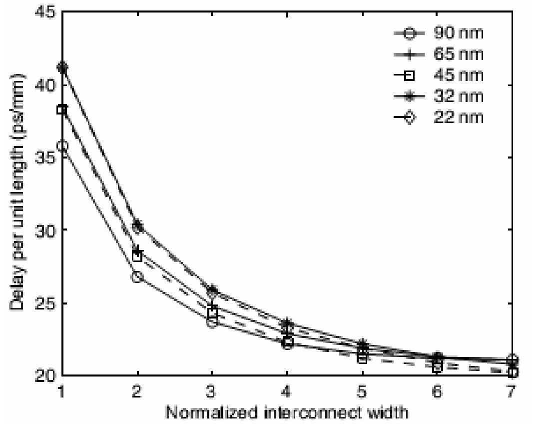


Fig.1 Minimum delay per unit length as a function of normalized interconnect with (W/W_{min}) [2].

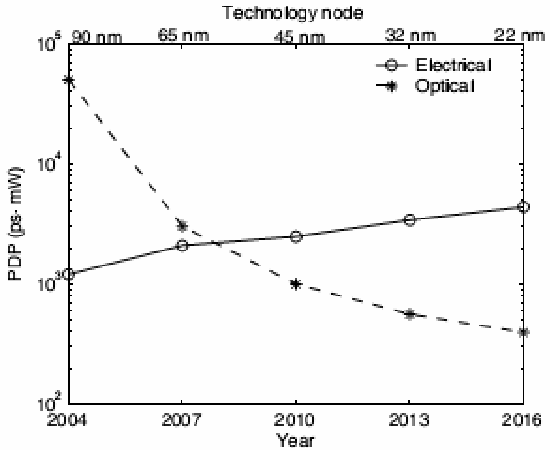


Fig.2 Power-Delay-Product (PDP) over technology node and year for 1cm length electrical and optical interconnects [2].

Electrical and Optical Interconnects

Challenges of electrical interconnects

- Wire/network delay
  - Dependency on distance and modulation frequency
  - Does not scale with the technology node [2]
- Power consumption
  - Increases with distance and bandwidth
  - Increasing power-delay product (Fig.2)
- Bandwidth density
  - Higher frequencies require wider pitch
  - Band-limited by Ball Grid Array (BGA)

Advantages of optical interconnects

- Fibre/network delay
  - No signal repeaters
  - Propagation speed independent from signal modulation frequency
- Power per Tera-Bit
  - ~50x lower than copper solution [1] (→chip cooling)
- Bandwidth density
  - Channel separation of a few microns enough
  - On- and Off-chip bandwidth identical
- Cost per Tera-Bit
  - ~50x less than copper solution [1]

[1] Proceedings of the IBM Printed Circuit Board Symposium, Raleigh, USA, 2011

[2] David A.B. Miller, „Rationale and Challenges for Optical Interconnects to Electronic Chips“, Invited Paper, Proceedings of the IEEE, Vol.88, No.6, June 2000

Silicon photonics

Requirements

- Compliance with
  - Standard Technology
  - Design methodology
  - CAD tools
- Reliable integration at standard cost
- Gain in performance

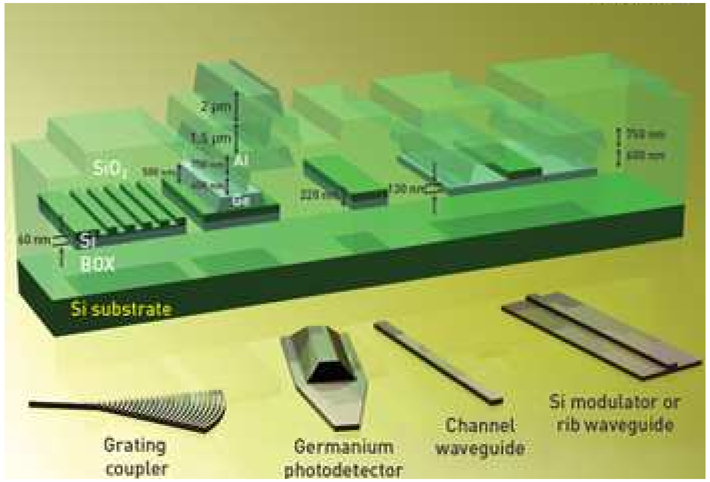


Fig.1 The main building Blocks for silicon photonic systems.
Source: Optics and Photonic News, 09/2013

Silicon is

...THE material in CMOS Technology
... optimal for waveguides
... not optimal for lasers or detectors

The challenge with silicon as absorbers

- Indirect bandgap
- Low absorption

Counter-measures

- Maximise depleted volume
- Optimize the optical path
- Light-trapping
- Avalanche effect

Polysilicon-Grating Detector (2007)

Challenges in a 45nm SOI technology

- Absorption length of silicon is ~5µm at 670nm
- Silicon channel is 70nm deep

Design Approach

- Polysilicon grating coupler to optimize the optical path
- Buried Oxide and Silicon Nitride to trap light

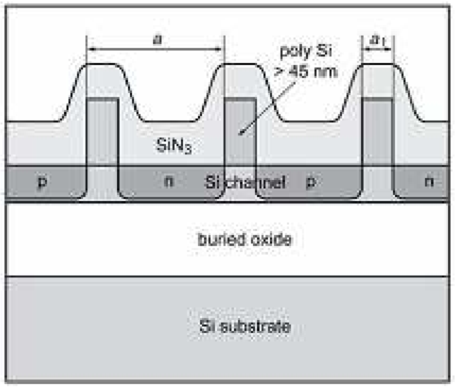


Fig.1 45nm CMOS SOI layers (side-view).

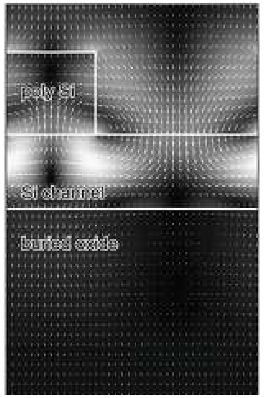


Fig.2 Intensity distribution and Poynting vector.

Optical simulation

- 6% absorption without grating
- 25% absorption with 1D-grating
- 66% absorption with 2D-grating

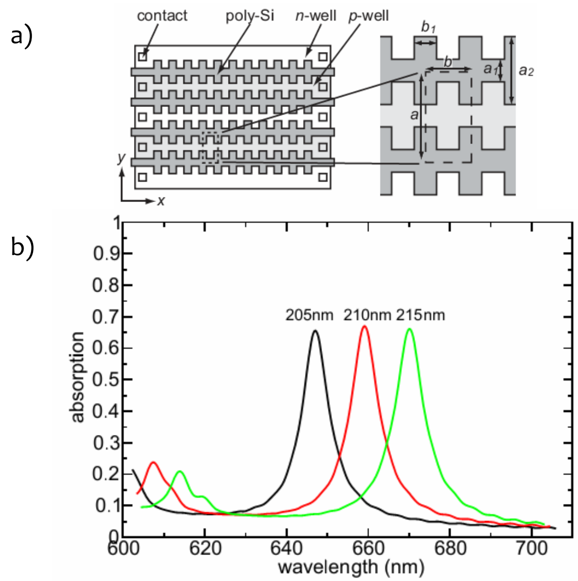


Fig.3 Combined absorption for s- and p-polarization (b) of a 2D grating (a) as a function of the wavelength for three different grating periods *a* (other parameters fix).

Polysilicon-Grating Detector

Measurement results

- Minmium rise time 8.5ps
  at 0.02 A/W responsitivity (f_{3dB} = 41GHz)
- Maximum responsitivity 0.07 A/W
  at 42ps rise time (f_{3dB} = 8.33GHz)
- Responsitivity of 2D-gratings about 3.3 times higher than for 1D-gratings

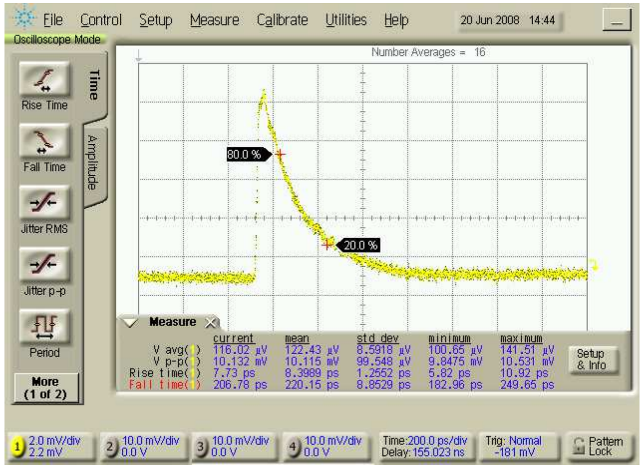


Fig.1 Impulse response of a 50x50 mm² detector measured with a 50GHz sampling oscilloscope and a 50 Ohm high speed waver probe.

Evaluation

- Good rise time
- Lower responsitivity than expected
- Deviation in peak wavelength

Reasoning

- Silicides (Nickel and Platinum)
- Process variations

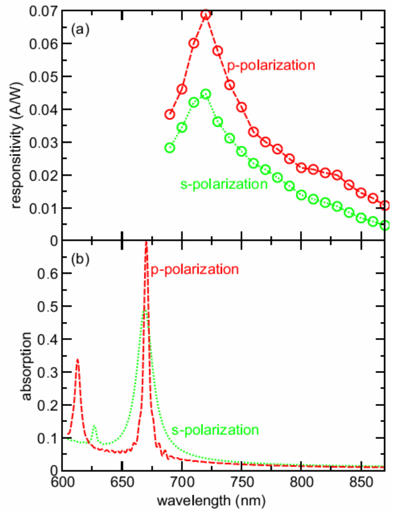


Fig.3 Simulated (bottom) and measured (top) absorption and responsitivity.

Shallow-Trench-Grating Detector (2009)

Challenges in a 32nm SOI technology

- Absorption length of silicon is ~15 µm at 850nm
- Silicon channel is 70nm deep
- Metal Gates (TiN)

Design Approach

- Shallow Trench Isolation (STI) grating
- P^-/N^+/STI structure in the silicon layer
- Large P^- regions to maximize intrinsic area

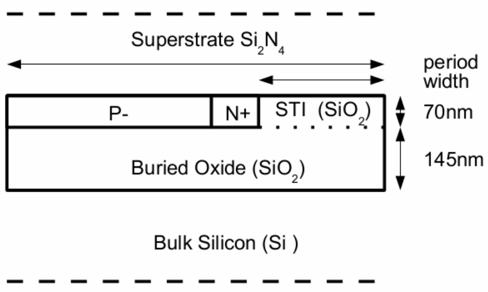


Fig.1 Side view on the Shallow-Trench grating with PIN-Diode.

Optical simulation

- 39.5% maximum absorption for TE-mode optimal period: 377nm
- 28.6% maximum absorption for TM-mode optimal period: 425nm
- 5% absorption loss within the accuracy of the semiconductor process

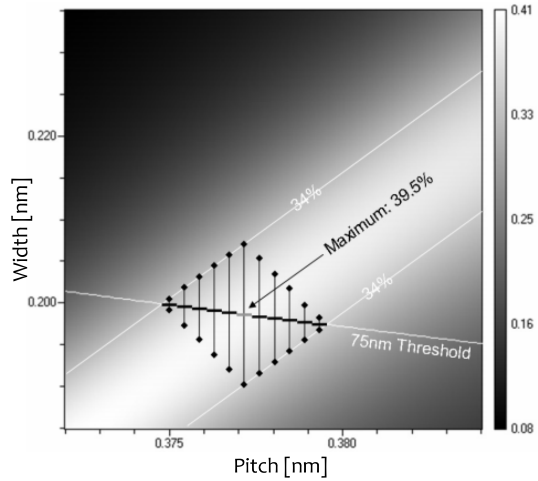


Fig.2 Grating period sensitivity analysis for a 5% drop in the bsorption.

Shallow-Trench-Grating Detector

Measurements

- Mean rise time 12ps and fall time <100ps at 0.05 A/W for a 25x25 μm² detector
- Maxmimum responsitivity 0.27 A/W for a 200x200 μm² detector
- Reverse bias of 4V

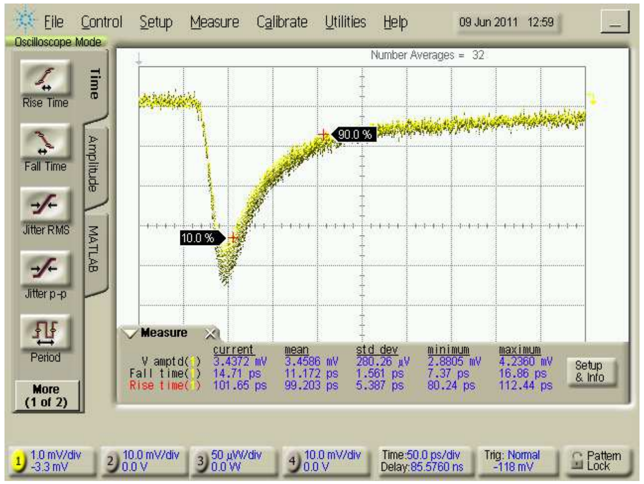


Fig.2 Impulse response of a 25x25μm2 detector (80 fs pulse, 80MHz rep-rate Ti-Sapphire laser).

Evaluation

- Very simple structure in standard CMOS SOI
- Improved rise time, fall time and responsitivity
- Alignment of peak absorption
- Sensitivity to variations in the CMOS process

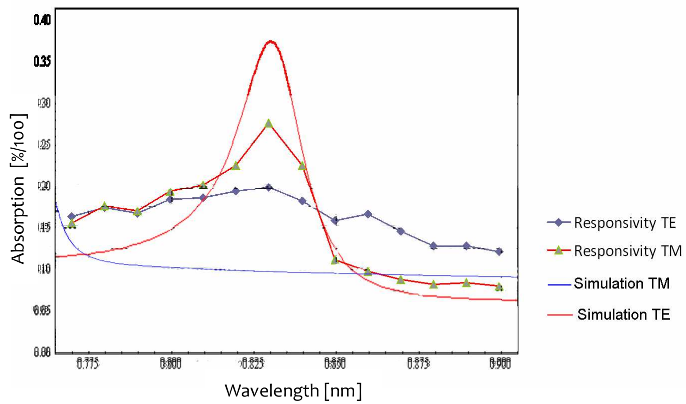


Fig.3 Simulation versus measured absorption.

Germanium waveguide detector (2011)

Design Approach

- IBM „Silicon-Nanophotonics Technology“ based on a 90nm CMOS process
- 20µm long and 100nm thick Germanium absorber
- Waveguide structure to feed detector with light
- Avalanche detector

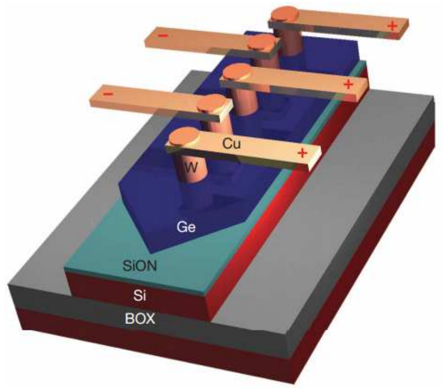


Fig.1 Structure of the Silicon-Germanium waveguide detector. Source: IBM Thomas J. Watson Research, J. Vlasov et al.

Results

- 0.5 A/W responsitivity at 1.3 µm and 1.5 µm
- 16ps rise and fall time
- 1.5V bias for 30 GHz with 10dB avalanche gain
- Bit Error Rate 10^{-12} and low noise up to 40GHz

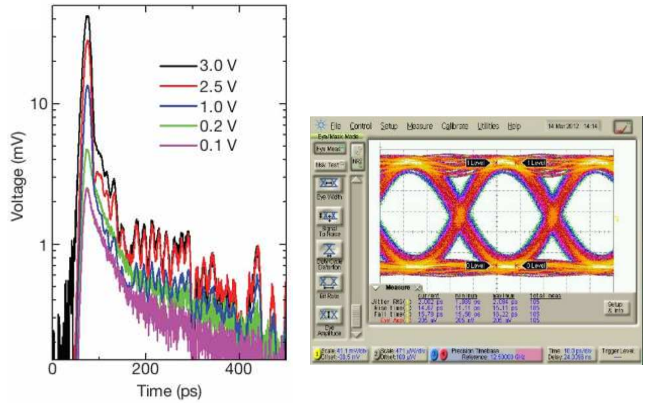


Fig.2 Semi-logarithmic plot of photocurrent transients and a variation in the bias voltage (left). Eye diagram at 40GHz (right).

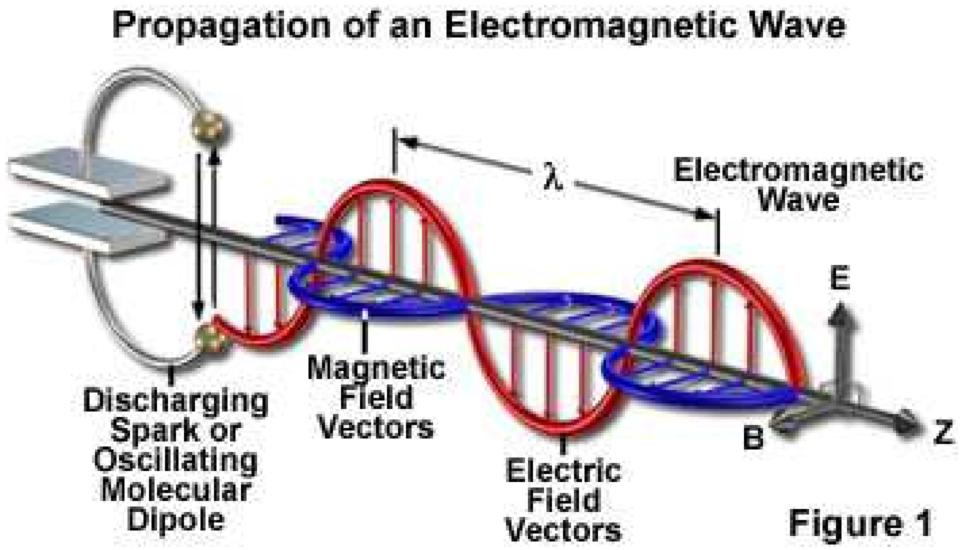
Summary

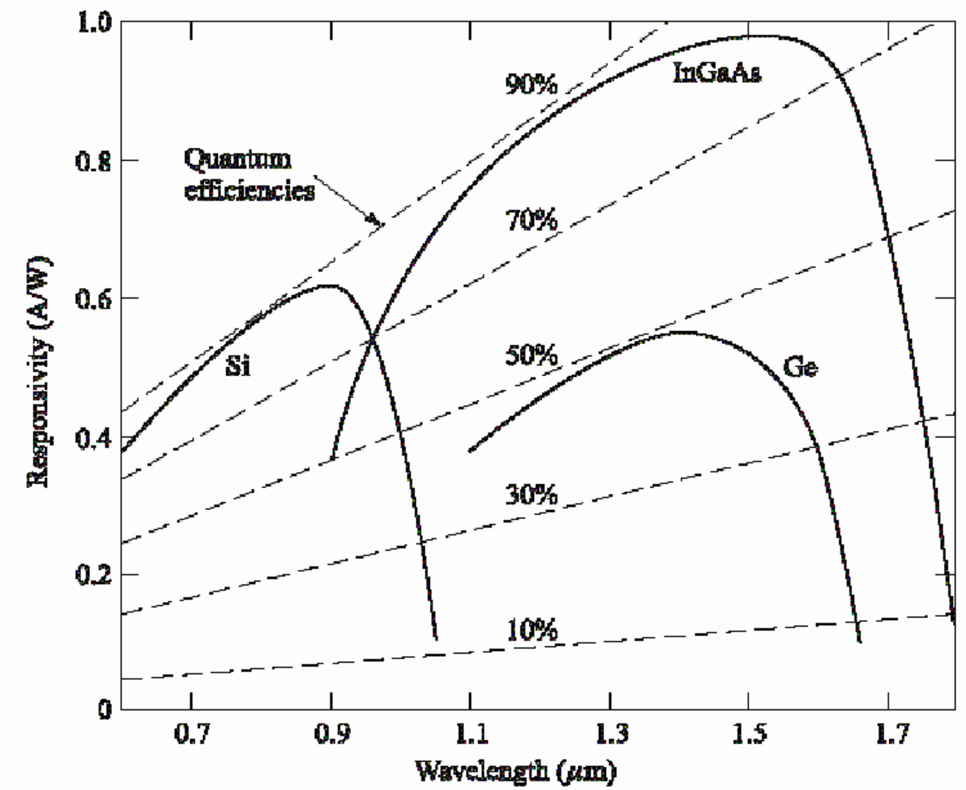
- Optimized gratings
  - enhance the local absorption (→proof of principle)
  - show a peak wavelength sparation a few nanometers (→WDM)
  - are sensitive to process variations (→process control)
- Grating enghanced detectors need quite large areas for reasonable responsitivities (→RC-delay)
- Germanium shows clear advantages due to optical properties

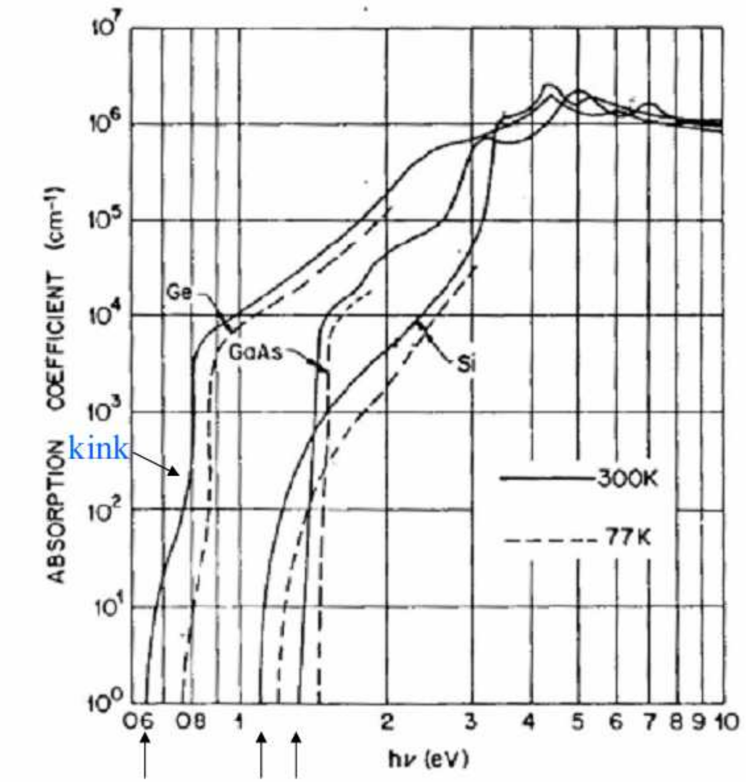
Outlook

- Silicon-Nano-Photonics is a young field of research with a wide range of applications and lots of opportunities
- We‘re today seeing just the first steps towards silicon-photonics in commercial products
- Optics and Electronics are moving closer together with a strong demand for engineers being experts in both domains

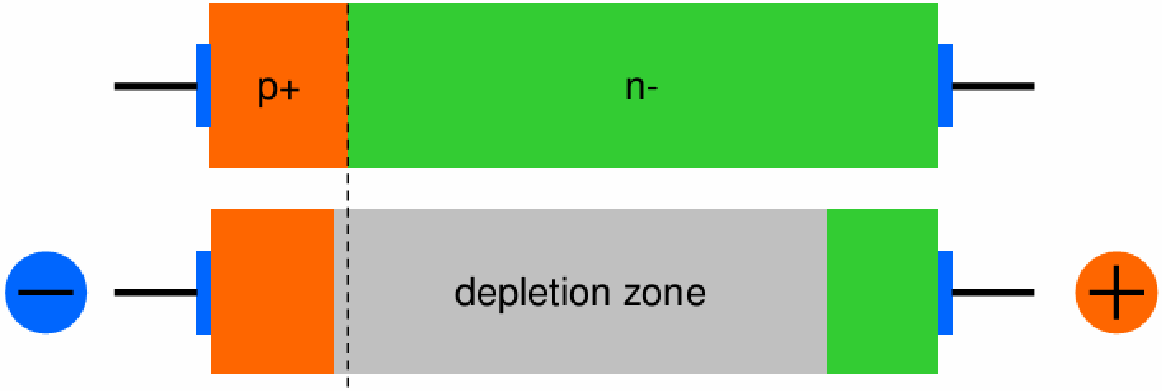
Thank you for your attention!


Propagation of an Electromagnetic Wave
λ
Electromagnetic Wave
E
Magnetic Field Vectors
Discharging Spark or Oscillating Molecular Dipole
Electric Field Vectors
B
Z
Figure 1





$$\text{AmperePerWatt} = \text{QE} \cdot \lambda \cdot q \,/\, h\, c$$



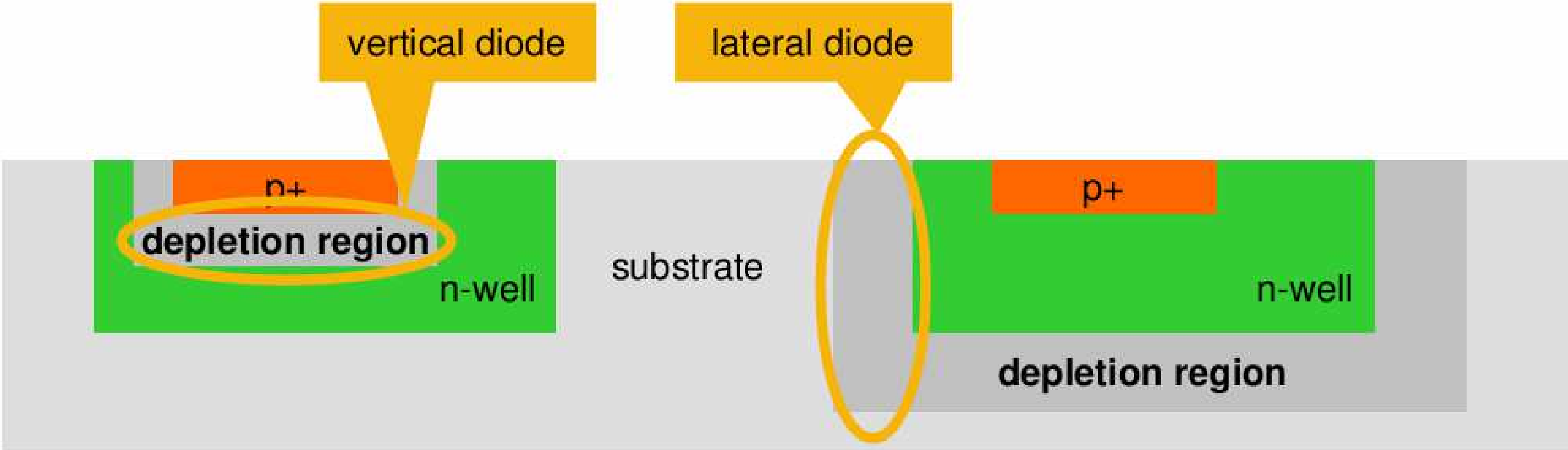
- A diode develops at every junction between p- and n-doped material.
- A **depletion zone** is created if a **reverse bias** is applied
- The depletion zone grows fast in **regions with low doping**
- The thickness grows often with the √ **of the applied voltage**
- The diode has a **capacitance** with **decreases with increasing bias**
- The fixed space charges in the depletion zone create an **electrical field**
- Photons absorbed in the depletion zone create **electron-hole pairs** which are separated by the field.
- Photons absorbed in the undepleted zones create e-h-pairs which diffuse around and either recombine, get trapped or ‘fall’ into the depletion zone. This is seen in dc-measurements.

- **Low doping** → thick depletion zone, small cap
- High bias → thick depletion zone, small cap, high field - fast!
- Close to surface → no loss ‘above’
- Large thickness → good absorption
- Large area → good light collection (only up to some limit!)

- Note:
  When diode area increases, capacitance also increases. There is no gain!
  Better concentrate available light intensity on small spot and **keep diode small**!

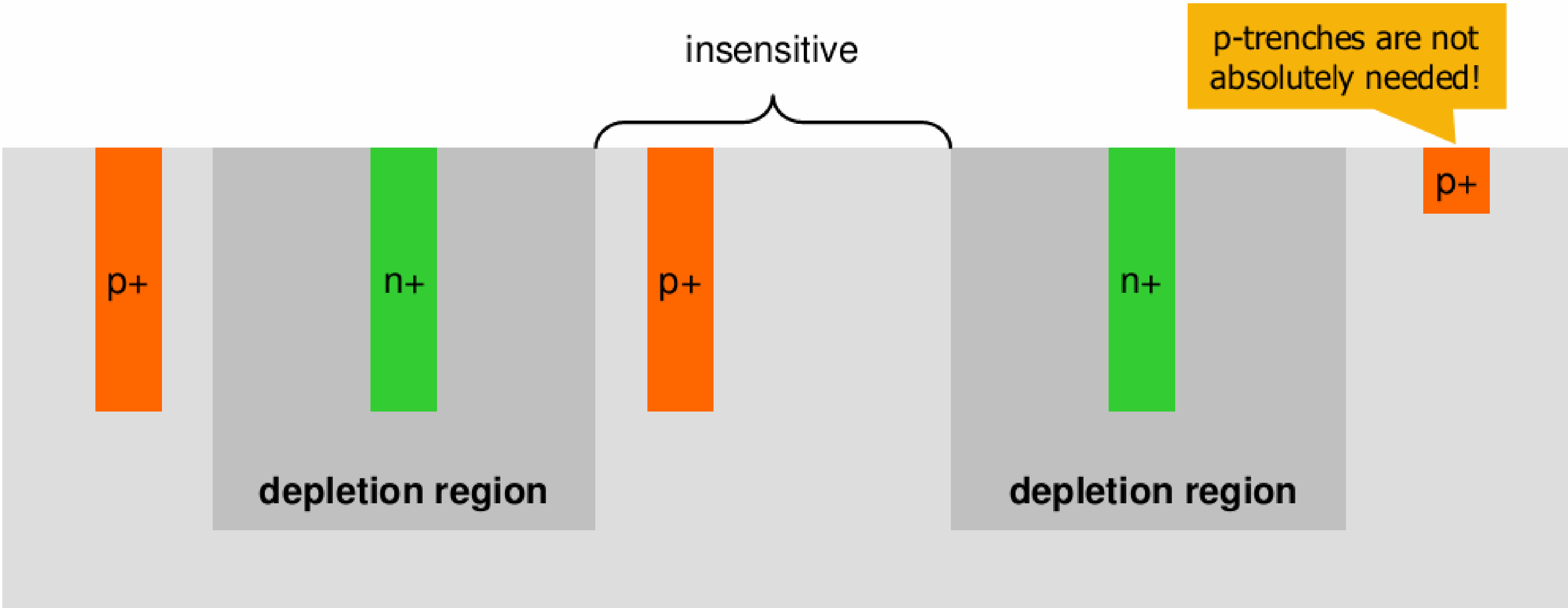
- Note:
  Depletion thickness for **fast** diodes may not be too thick, because charge collection needs some time: electrons in a 3.3µm thick diode at 3.3V bias need ~ 30ps for collections. And holes are x3 slower…. (Also watch velocity saturation!)

- Examples of diodes in CMOS technology:



for low doped n-well
read out at p+ (smaller cap!)

for low doped substrate
readout at nwell (substrate = gnd)



- Must chose pitch ≤ depletion thickness to avoid insensitive area
- When is trench diode better?
  → when trenches are deeper than depletion thickness, i.e. in highly doped substrate (but: capacitance of these diodes is high – better use shallow trenches then…)
- Note: 'deep' trench diodes are faster than 'thick' vertical diodes!

The ***quantum efficiency*** (***external quantum efficiency***) η of a photodetector is the probability that a single photon incident on the device generates a photocarrier pair that contributes to the detector current.

$$\eta(\lambda) = \zeta\,(1\text{-}R)\,[1 - \exp(-\alpha(\lambda)d)]$$

R is the optical power reflectance at the surface, ζ is the fraction of electron-hole pairs that contribute to the detector current, $\alpha(\lambda)$ the absorption coefficient of the material, and d the photodetector depth.

ζ is the fraction of electron-hole pairs that *avoid recombination (often dominated at the material surface)* and contribute to the useful photocurrent. *Surface recombination* can be reduced by careful material growth and device design/fabrication.

$[1 - \exp(-\alpha(\lambda)d)]$ represents the fraction of the photon flux absorbed in the bulk of the material. The device should have a value of d that is *sufficiently large*. ($d > 1/\alpha$, $\alpha = 10^4\ \mathrm{cm}^{-1}$, $d > 1\ \mu\mathrm{m}$)